RGB/LVDS-to-eDP Converter

1 Features

Embedded-DisplayPort (eDP) Output

1/2/**4-lane** eDP @ 1.62/2.7Gbps per lane
HD to WQXGA **(2560*1600)** supported
Up to 6dB pre-emphasis

RGB Input

18/24bit RGB Interface
Pixel clock up to 270MHz
SDR/DDR supported
Pin order reversal supported

LVDS Input

Single/Dual-channel 6/8bit LVDS (Sync) interface
400Mbps to 1Gbps per data pair
Built-in termination
Channel and polarity swap supported

Reference Clock

Any freq. between 19MHz and 100MHz
Crystal or single-ended clock input
Built-in 5000ppm SSC generator

Misc

I^2C for chip configuration
Built-in eDP handshake protocol
I^2C-AUX channel for TCON/DPCD/EDID control
Built-in video test pattern

Power

1.2V core supply
2.5V or 3.3V IO supply
RGB IO can go down to 1.8V
Power consumption ~ 100mW
@ 2048*1536*24bit*60Hz, LVDS mode
Deep-sleep mode power <1mW

Package

QFN-56 (7mm x 7mm) package
RoHS Compliant
Sample available now

2 Block Diagram